CLAIMS

I/We claim:

[c1] 1. A method of forming nonvolatile memory, said method comprising:

providing a semiconductor substrate having gate dielectric layer formed thereon, a conductive layer formed on said gate dielectric layer and a first photo-resist pattern formed on said conductive layer;

etching said gate dielectric and said conductive layer to form a gate on said semiconductor substrate using said first photo-resist pattern as an etching mask;

removing said first photo-resist pattern;

patterning a second photo-resist pattern on said semiconductor substrate to expose selected side of said semiconductor substrate;

performing a first ion implantation to implant ions into said selected side of said semiconductor substrate to form a first implanted region by using said second photo-resist pattern as a code implanting mask.

[c2] 2. The method of Claim 1, further comprising forming silicide on said first implanted region.

[c3] 3. The method of Claim 1, wherein said gate dielectric layer includes oxide.

[c4] 4. The method of Claim 3, wherein said oxide includes silicon dioxide.

[c5] 5. The method of Claim 1, wherein said gate dielectric layer is formed by the material with high dielectric constant.

[c6] 6. The method of Claim 5, wherein said dielectric constant is around 3-100.

[c7] 7. The method of Claim 5, wherein said material with high dielectric constant is selected from Ta_2O_5, Al_2O_3, ZrO_2, HfO_2, Gd_2O_3 or Y_2O_3.

[c8] 8. The method of Claim 1, wherein the ion source for said first ion implantation is selected from the group consisting of phosphorus, arsenic, boron and the combination thereof.

[c9] 9. The method of Claim 1, further comprises a step of performing an optional pocket ion implantation after the formation of said gate, wherein the conductive type of said pocket ion implantation region is opposite to the one of said first implanted region.

[c10] 10. A method of forming nonvolatile memory, said method comprising:

providing a semiconductor substrate having gate dielectric layer formed thereon, a conductive layer formed on said gate dielectric layer and a first photo-resist pattern formed on said conductive layer;

etching said gate dielectric and said conductive layer to form a gate on said semiconductor substrate using said first photo-resist pattern as an etching mask;

removing said first photo-resist pattern;

patterning a second photo-resist pattern on said semiconductor substrate to expose selected side of said gate;

performing a first ion implantation to implant ions into said selected side of said gate to form a first implanted region by using said second photo-resist pattern as an implanting mask;

removing said second photo-resist pattern;

forming an isolation layer onto said gate;

forming spacers attached on sidewalls of said isolation layer;

performing a second ion implantation to implant ions into said semiconductor substrate to form second implanted regions by using said gate and said spacers as an implanting mask.

[c11] 11. The method of Claim 10, wherein said gate dielectric layer includes oxide.

[c12] 12. The method of Claim 11, wherein said oxide includes silicon dioxide.

[c13] 13. The method of Claim 10, wherein said gate dielectric layer is formed by the material with high dielectric constant.

[c14] 14. The method of Claim 13, wherein said dielectric constant is around 3-100.

[c15] 15. The method of Claim 13, wherein said material with high dielectric constant is selected from Ta_2O_5, Al_2O_3, ZrO_2, HfO_2, Gd_2O_3 or Y_2O_3.

[c16] 16. The method of Claim 10, wherein said isolation layer and spacers are formed of the material selected from oxide, nitride or the combination thereof.

[c17] 17. The method of Claim 10, wherein the ion source for said first and said second ion implantations is selected from the group consisting of phosphorus, arsenic, boron and the combination thereof.

[c18] 18. The method of Claim 10, further comprises a step of performing an optional pocket ion implantation after the formation of said gate, wherein the conductive type of said pocket ion implantation region is opposite to the one of said first and second implanted regions.

[c19] 19. A nonvolatile memory, comprising:

a substrate having source/drain formed at unselected side and source/drain with extension source/drain formed at other selected side;

gate dielectric layer formed on said substrate;

gate formed on said gate dielectric layer;

isolation layer formed along the surface of said gate;

spacers formed attached on the sidewalls of said isolation layer.

[c20] 20. The nonvolatile memory of Claim 19, wherein the thickness of said gate is approximately 800-2500 angstroms.

[c21] 21. The nonvolatile memory of Claim 19, wherein the thickness of said gate dielectric layer is approximately 10-250 angstroms.

[c22] 22. The nonvolatile memory of Claim 19, wherein the thickness of said isolation layer is approximately 20-200 angstroms.

[c23] 23. The nonvolatile memory of Claim 19, wherein the width of said spacers are approximately 200-2000 angstroms.

[c24] 24. The nonvolatile memory of Claim 19, further comprising silicide on said gate, first and source/drain regions.

[c25] 25. The nonvolatile memory of Claim 19, wherein said gate dielectric layer includes oxide or the material with high dielectric constant.

[c26] 26. The nonvolatile memory of Claim 25, wherein said dielectric constant of said high dielectric constant is around 3-100.

[c27] 27. The nonvolatile memory of Claim 26, wherein said material with high-k (dielectric constant) is selected from Ta_2O_5, Al_2O_3, ZrO_2, HfO_2, Gd_2O_3 or Y_2O_3.

[c28] 28. The nonvolatile memory of Claim 19, wherein said spacers are formed of the material selected from oxide, nitride or the combination thereof.

[c29] 29. The nonvolatile memory of Claim 19, wherein the ion source for said source/drain is selected from the group consisting of phosphorus, arsenic, boron and the combination thereof.

[c30] 30. The nonvolatile memory of Claim 19, further comprises a pocket ion implantation region formed adjacent to said gate or source/drain, wherein the conductive type of said pocket ion implantation region is opposite to the one of said source/drain.

[c31] 31. A method of operating a nonvolatile memory during reading mode, wherein said nonvolatile memory includes a gate formed on a substrate, said gate having a first spacer formed on a first sidewall of said gate and a second spacer formed on a second sidewall of said gate, a first source/drain region formed in a first side of said substrate, a second source/drain region formed in a second side of said substrate, an impurity extension region selectively formed adjacent to either said first or said second source/drain regions or none or both, said method comprising:

applying a gate bias on said gate;

applying a first bias on said first source/drain and applying a second bias on said second source/drain thereby causing the current to be read indicating the presence or absence of said impurity extension region located under said first spacer, which is defined as the first digital status;

applying a third bias on said first source/drain and applying a fourth bias on said second source/drain thereby cause the current to be read indicating the presence or absence of said impurity extension region located under said second spacer, which is defined as the second digital status.

[c32] 32. The method of Claim 31, wherein said first bias is grounded or approximately closer to ground potential than said second bias.

[c33] 33. The method of Claim 31, wherein said fourth bias is grounded or approximately closer to ground potential than said third bias.

[c34] 34. The nonvolatile memory of Claim 31, further comprises a pocket ion implantation region formed adjacent to said gate or said source/drain regions, wherein the conductive type of said pocket ion implantation region is opposite to the one of said source/drain regions.